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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

ATTY.'S DOCKET: FRIEDMAN =2

In re Application of:	)	Confirmation No.: 4467
Rogi FRIEDMAN	)	
Appln. No.: 09/893,543	)	Art Unit: 2634
Filing Date: June 29, 2001	)	Examiner: Eva Zheng
For: METHOD AND SYSTEM FOR...	)	May 25, 2005

COMMENTS ON STATEMENT FOR REASONS FOR ALLOWANCE

Honorable Commissioner for Patents
U.S. Patent and Trademark Office
Customer Service Window
Randolph Building, Mail Stop Issue Fee
401 Dulany Street
Alexandria, VA 22314

Sir:

Applicant does not entirely agree with the Statement for Reasons for Allowance attached to the Notification of Allowability mailed April 5, 2005, particularly due to certain clerical and/or typographical errors and the inclusion of certain redundant and/or extraneous terminology in such Statement. Accordingly, applicant submits that the Statement of Reasons for Allowance should be corrected to read as follows (wording to be deleted being stricken through, and wording to be added being underlined):

None of the prior art teaches or suggests ~~that~~ a method and a device for fast ~~and~~ synchronization of multiframe structures~~. Detecting~~ by detecting a period binary signature in a binary signal transmitted at a particular bit rate. The signature forming a pre-selected binary code having a code length of "C" binary symbols spread over the signal with a known spacing "D" of bits between the binary symbols of the signature as well as between adjacent signatures; the device comprising: a state machine including a logical scheme interconnected with a memory block, the memory block of the state machine comprising "D" independent memory cells each having its serial number, the memory cells being cyclically connectable to the logical scheme; each of the memory cells, when in conjunction with the logical scheme, being capable of registering "K" successive binary states of the state machine including an initial state and a terminal state; "K" states comprising "C" successive binary states respectively associated with "C" binary symbols of the code successively appearing in said signature; a control unit responsible for switching said logical scheme to D memory cells according to their serial numbers and in a cyclical manner at a rate equal to the bit rate of said signal so that, a different memory cell is connected to the logic scheme at each of the time clocks within a group of D time clocks, the control unit being further capable of continuously checking whether at least one cell of the "D" memory cells has registered the terminal state, and of selecting therefrom a single one considered as detecting the signature; the

arrangement being such that, if one and the same initial binary state is assigned to all the cells in the memory block, and if said binary signal is applied to the state machine at its bit rate, each bit in any group D successive bits of the binary signal will be processed using a particular cell of the memory cells, thereby associating each of the memory cells with a particular bit in any group of D successive bits and allowing a periodic signature ~~formed by a particular bit within said successive bits~~ to be detected by the respective particular memory cell of D cells, wherein: "C" - is an integer which is a number of binary positions of the periodic binary signature, "D" - is an integer, the integer being a) a number f binary positions of the binary signal forming the spacing between adjacent binary symbol of the periodic binary signature, and b) a number of independent memory cells, "K" - is an integer which is a number of successive binary states of the state machine, "K" being no less than "C'.

Please enter the corrected version above.

Respectfully submitted,

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